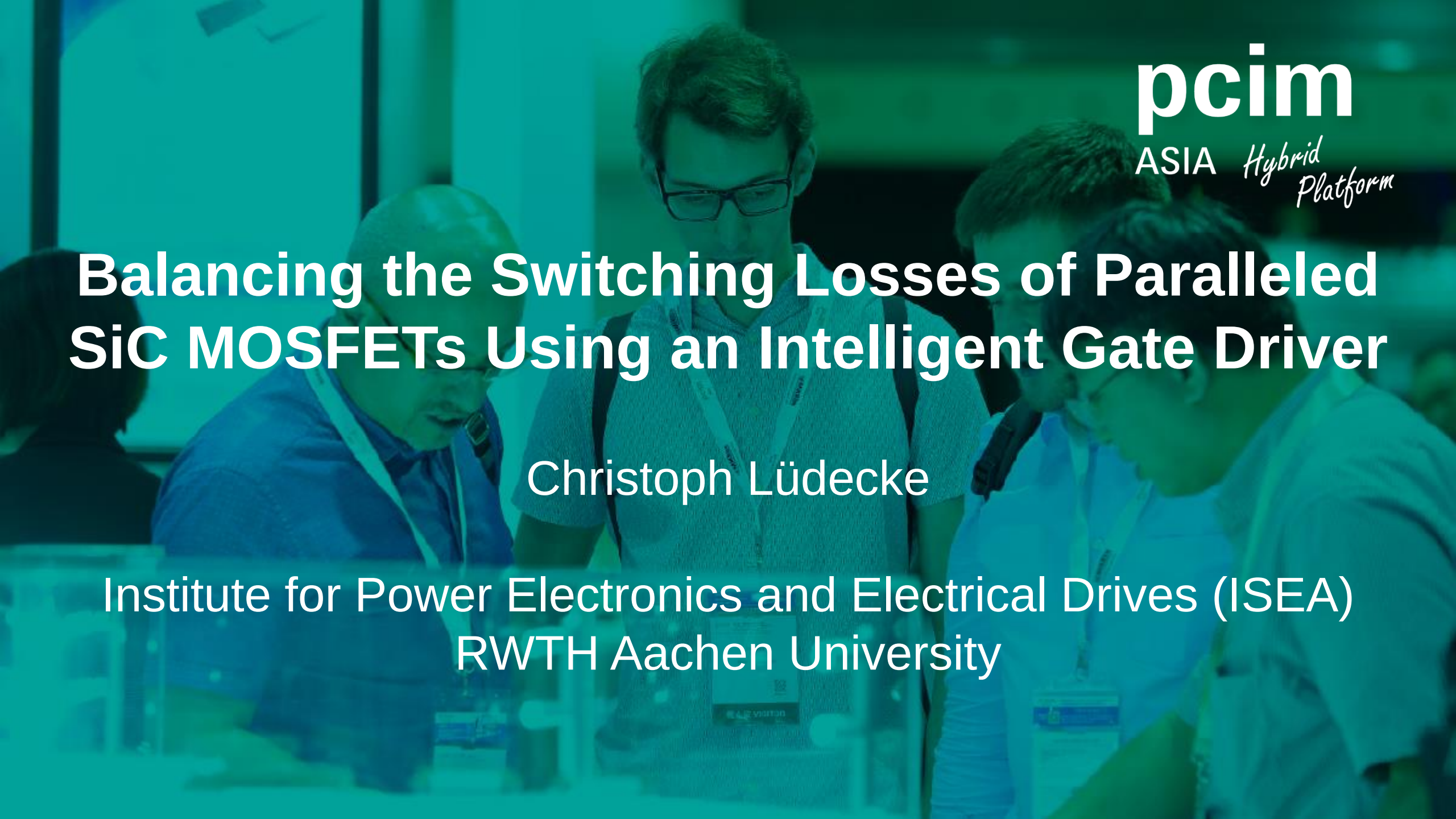

pcim ASIA Hybrid Platform

Balancing the Switching Losses of Paralleled SiC MOSFETs Using an Intelligent Gate Driver

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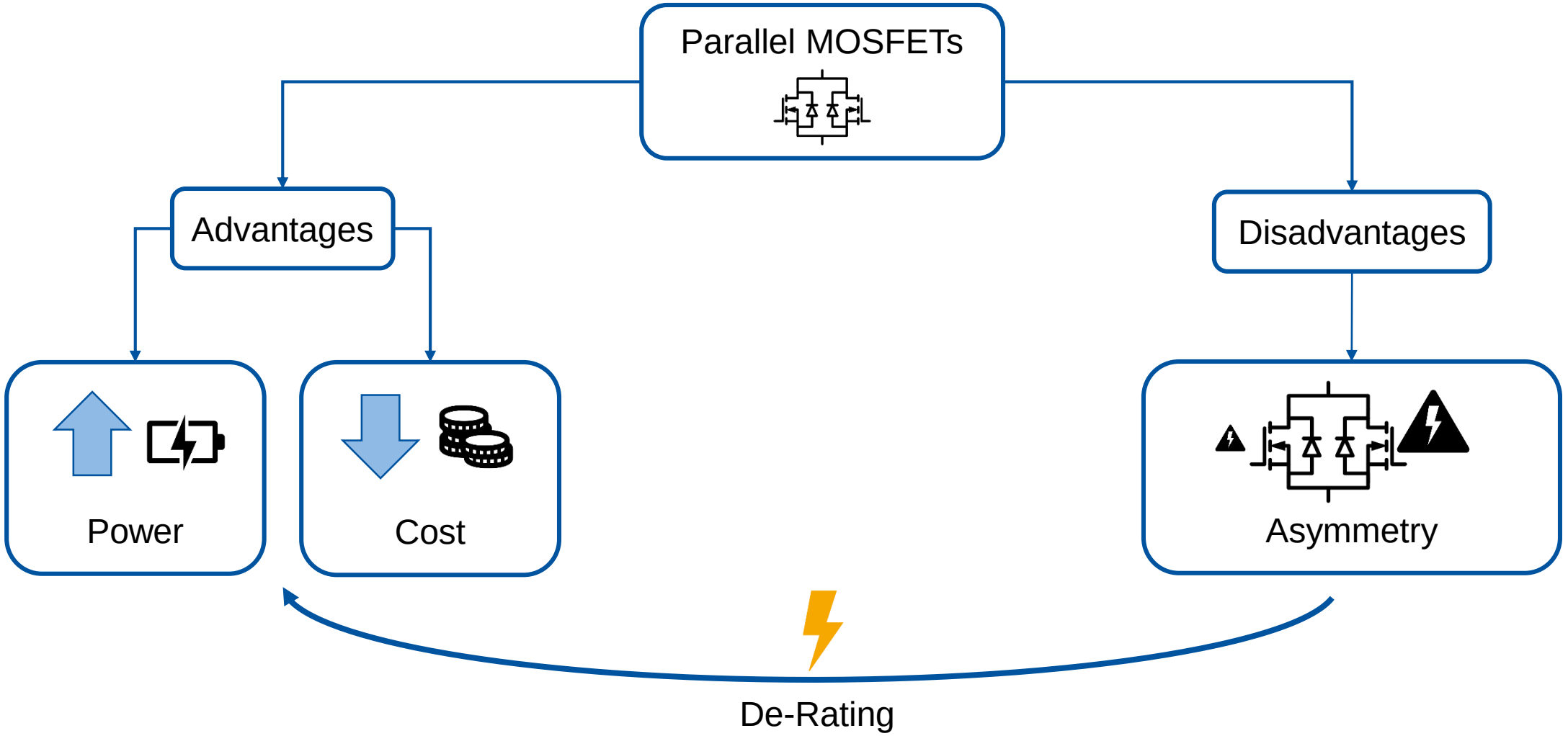
Motivation


Parallel MOSFETs
Advantages
Disadvantages
Power
Cost
Asymmetry
De-Rating

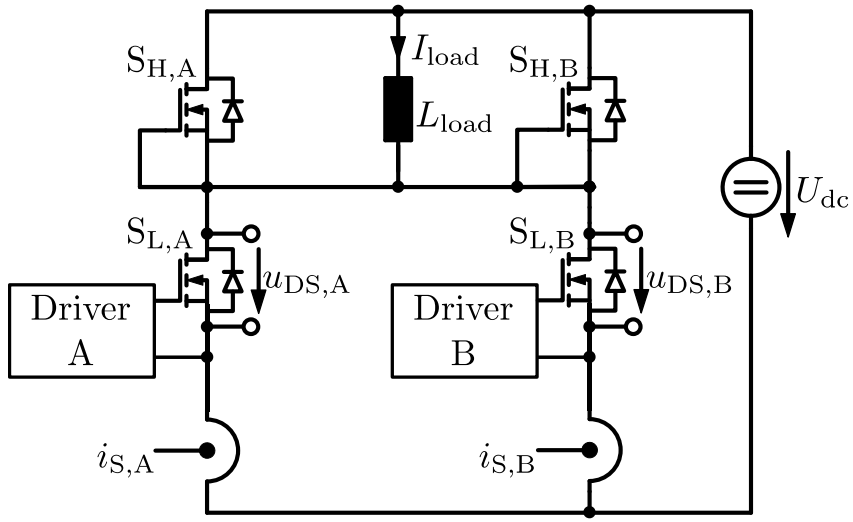
Content

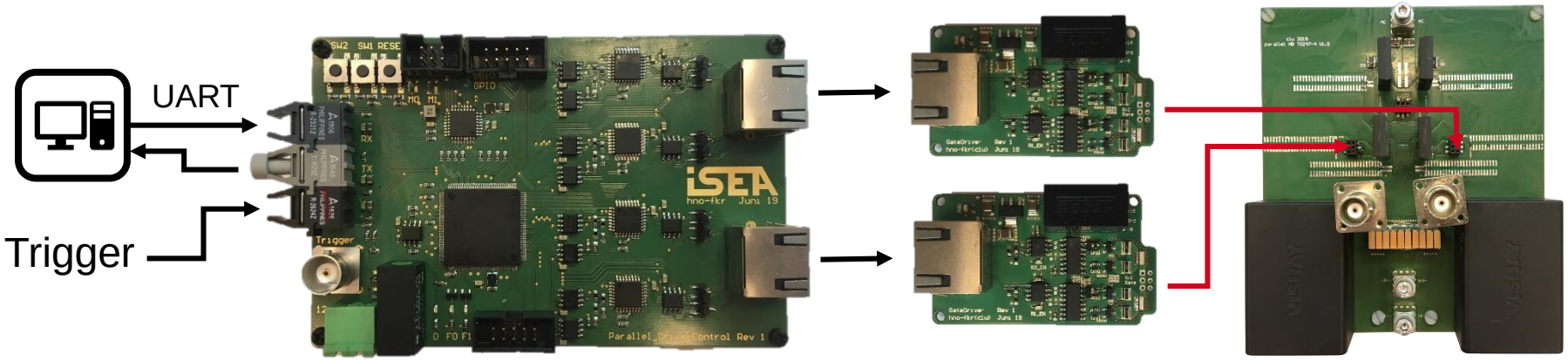
- Motivation

- Test Setup
- Influence of Gate Delay on Current Transients
  - Turn-on
  - Turn-off
- Conclusion & Outlook

Test Setup

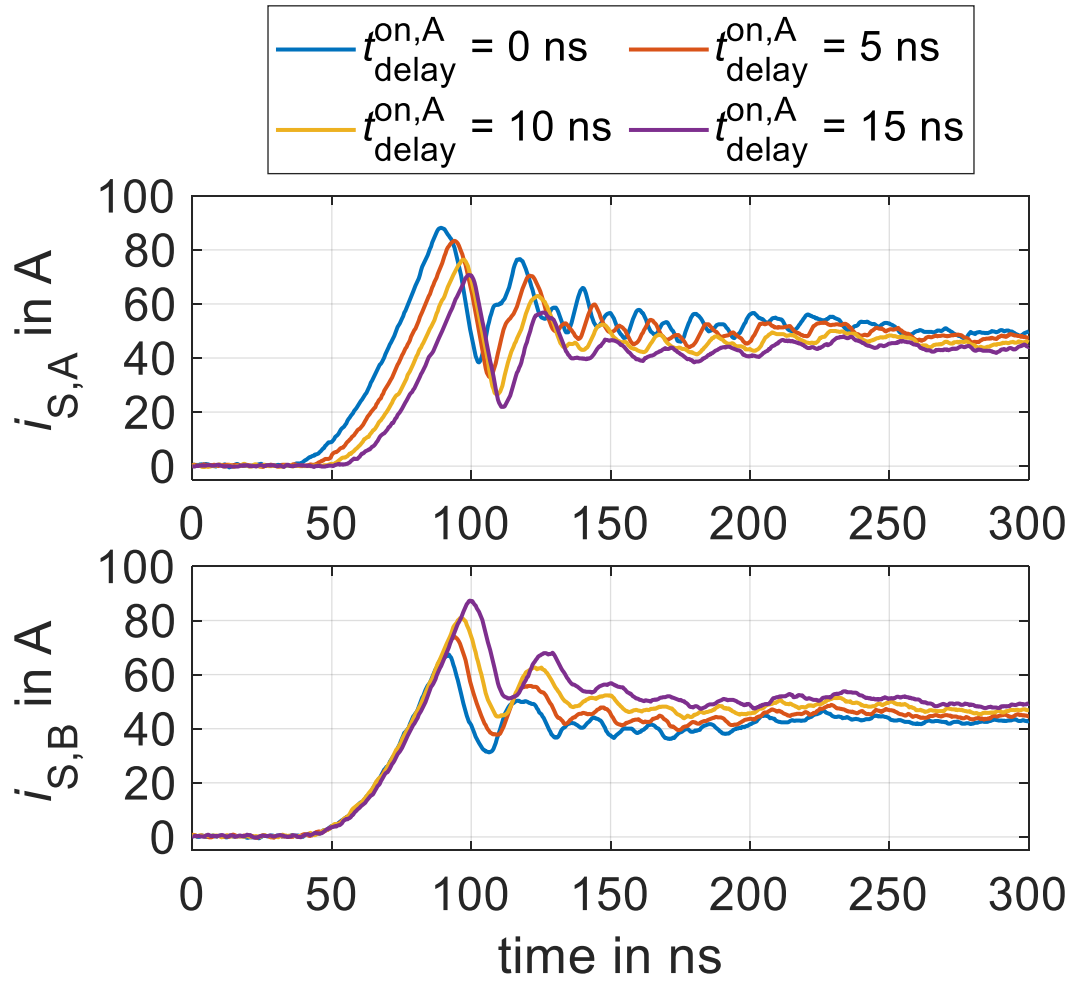
- Two parallel half bridges
  - 50 A, 1200 V per MOSFET
- Galvanically isolated gate driver for each low-side MOSFET
- FPGA controls gate signal delay
  - 0 ns … 20 ns delay with 10 ps resolution

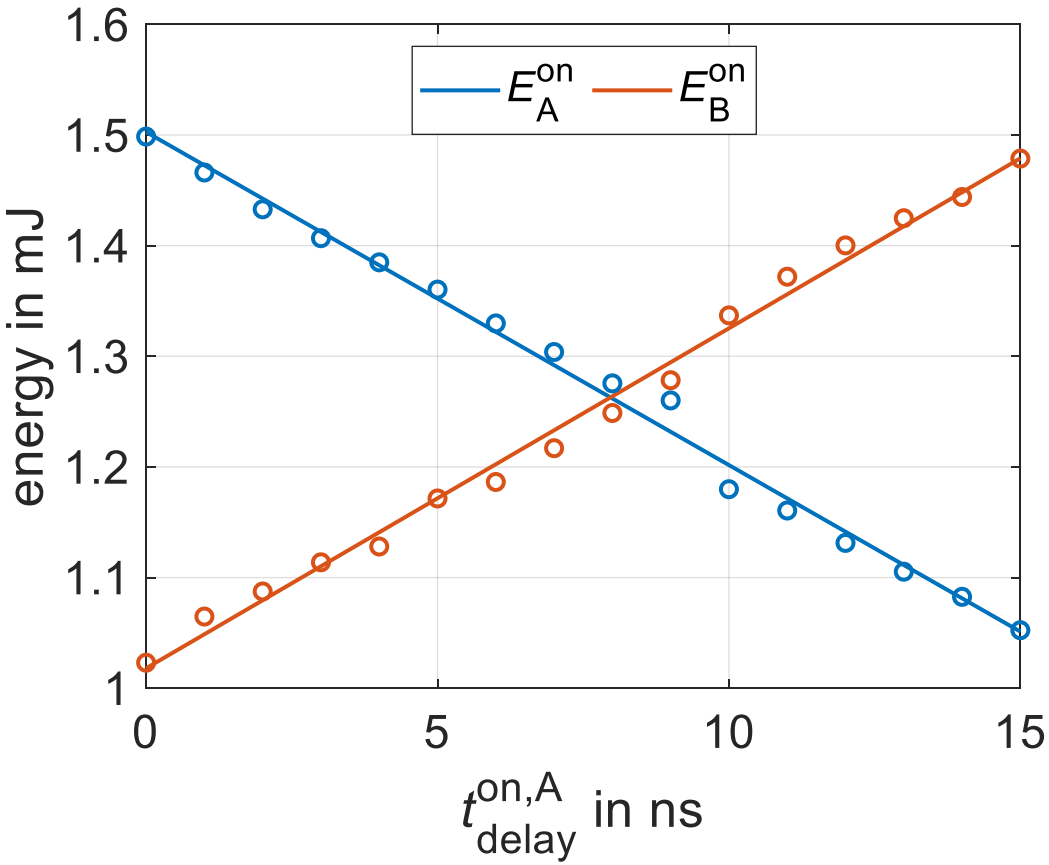




Control PCB | Gate driver | Half bridge

Influence of Gate Delay on Current Transients
Turn-on





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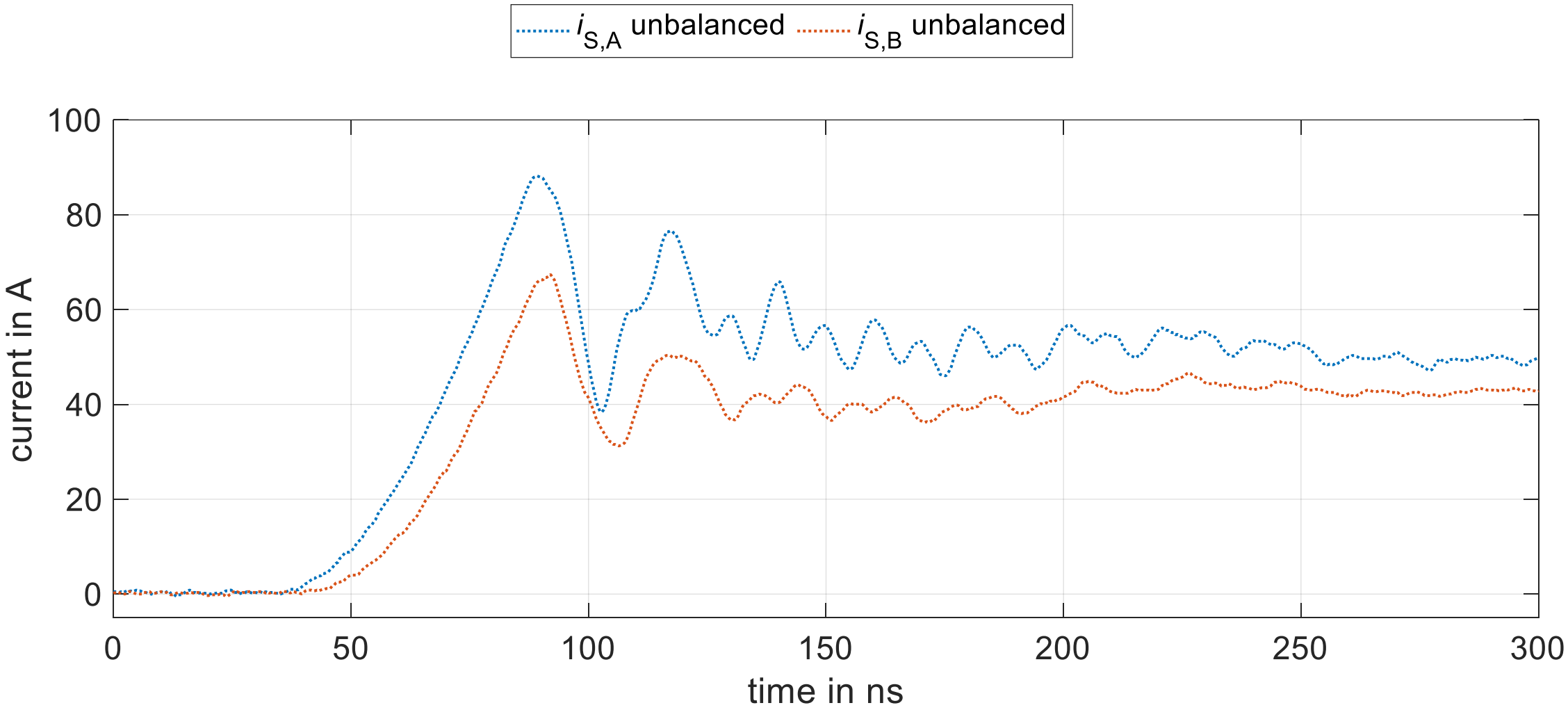
Influence of Gate Delay on Current Transients
Turn-on



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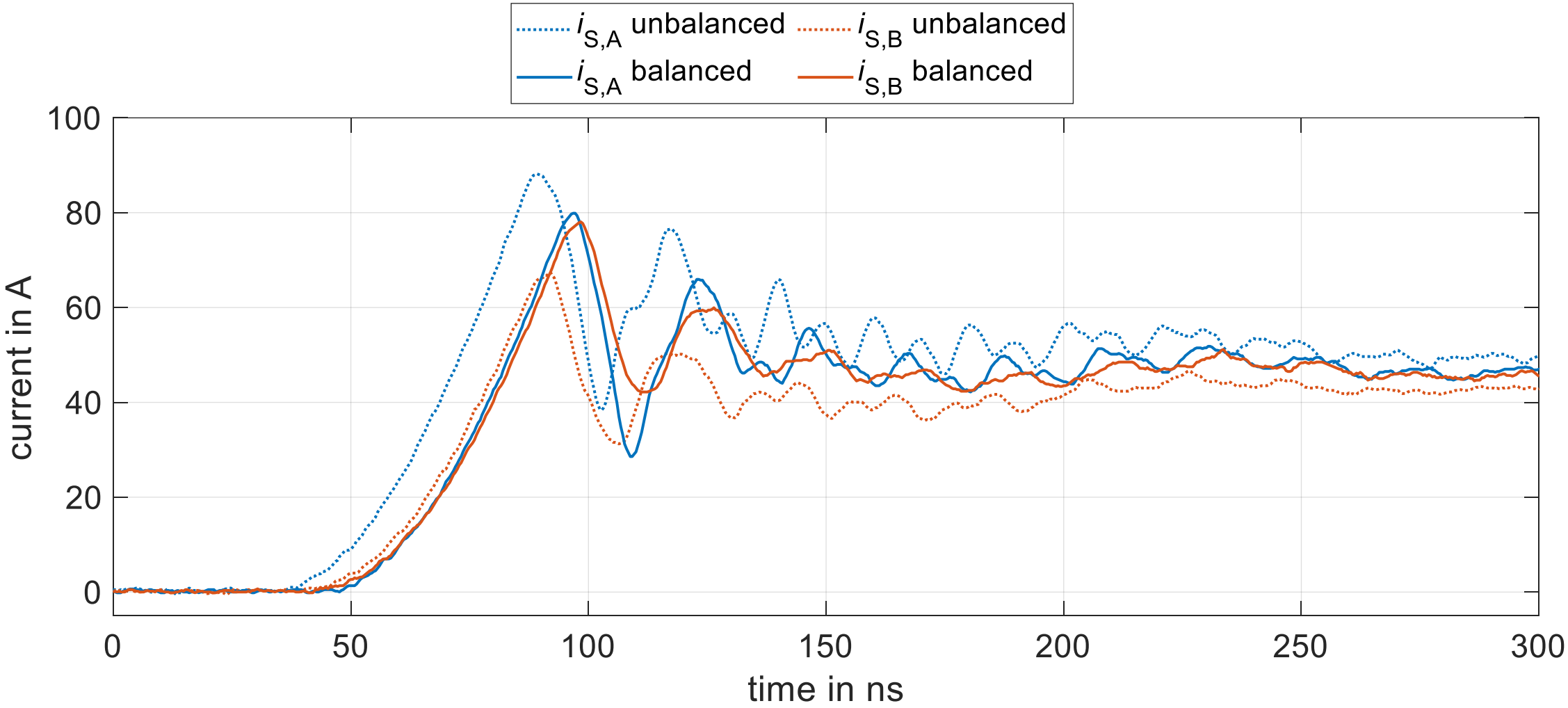
Influence of Gate Delay on Current Transients
Turn-on



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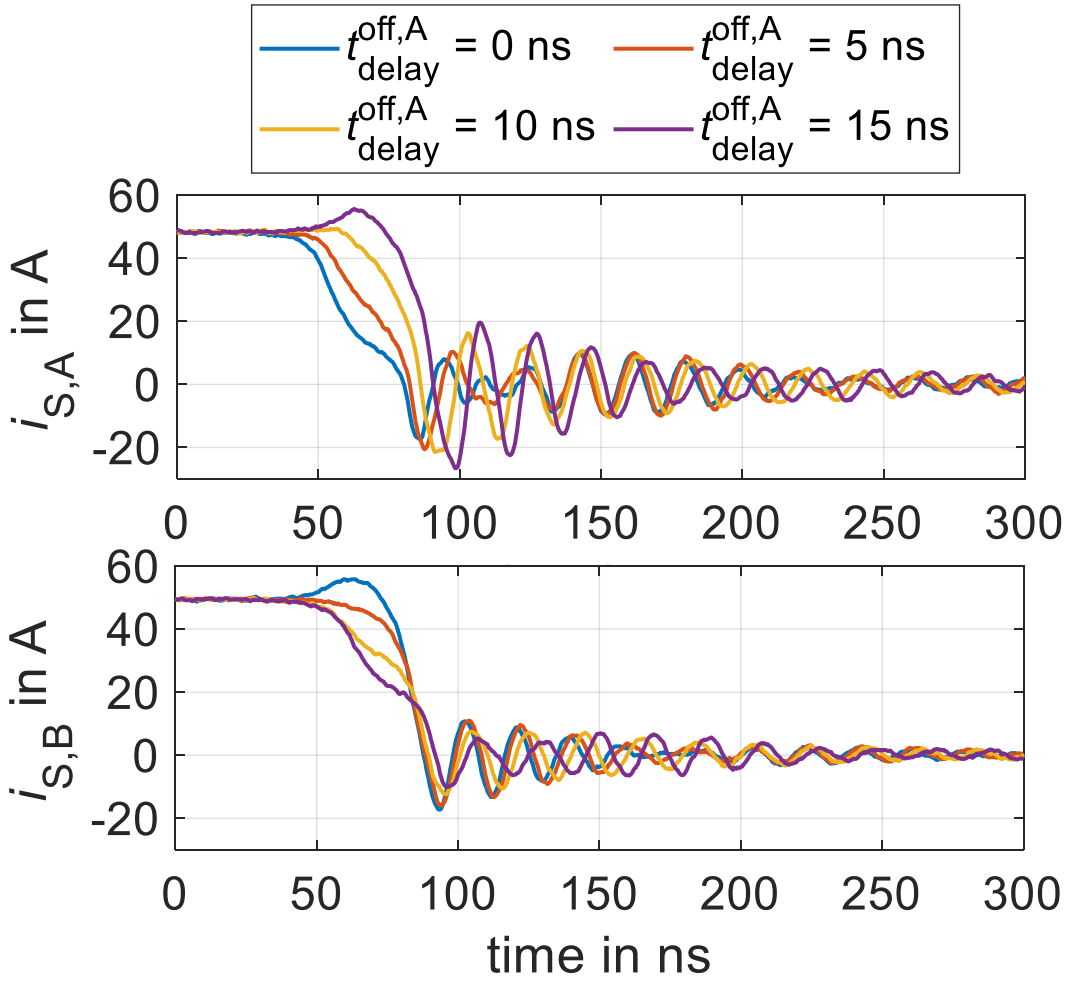
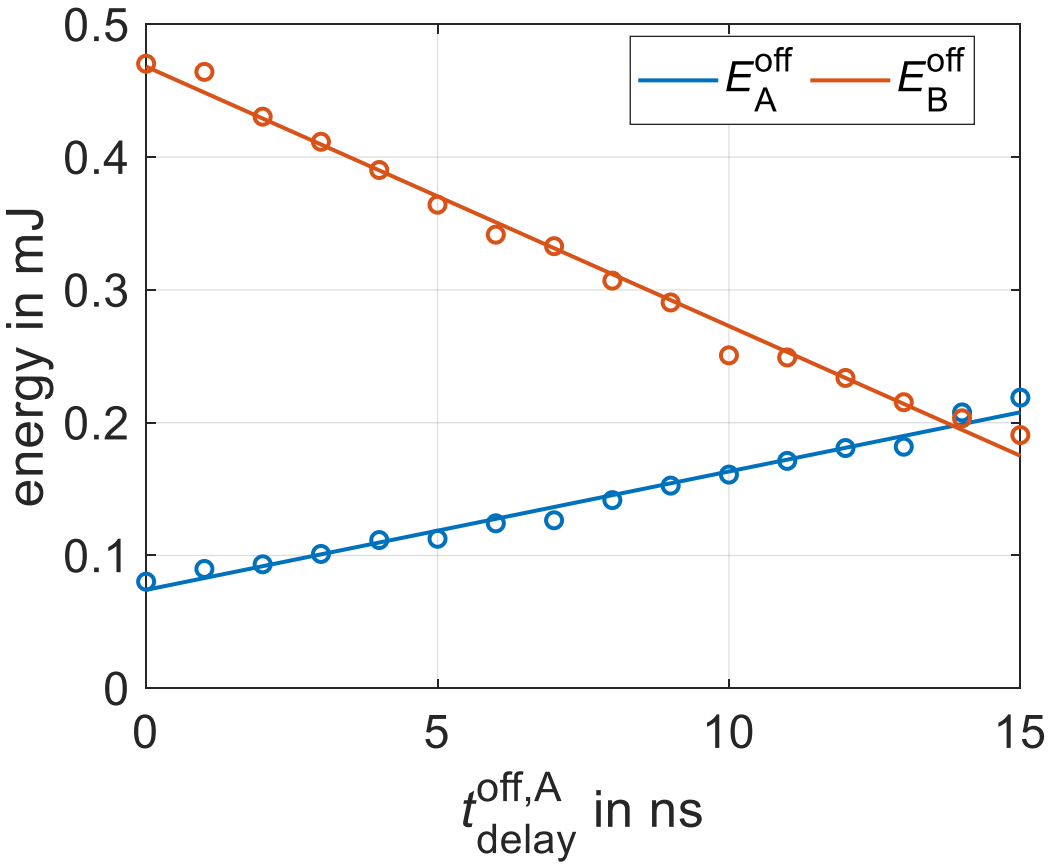
Influence of Gate Delay on Current Transients
Turn-off





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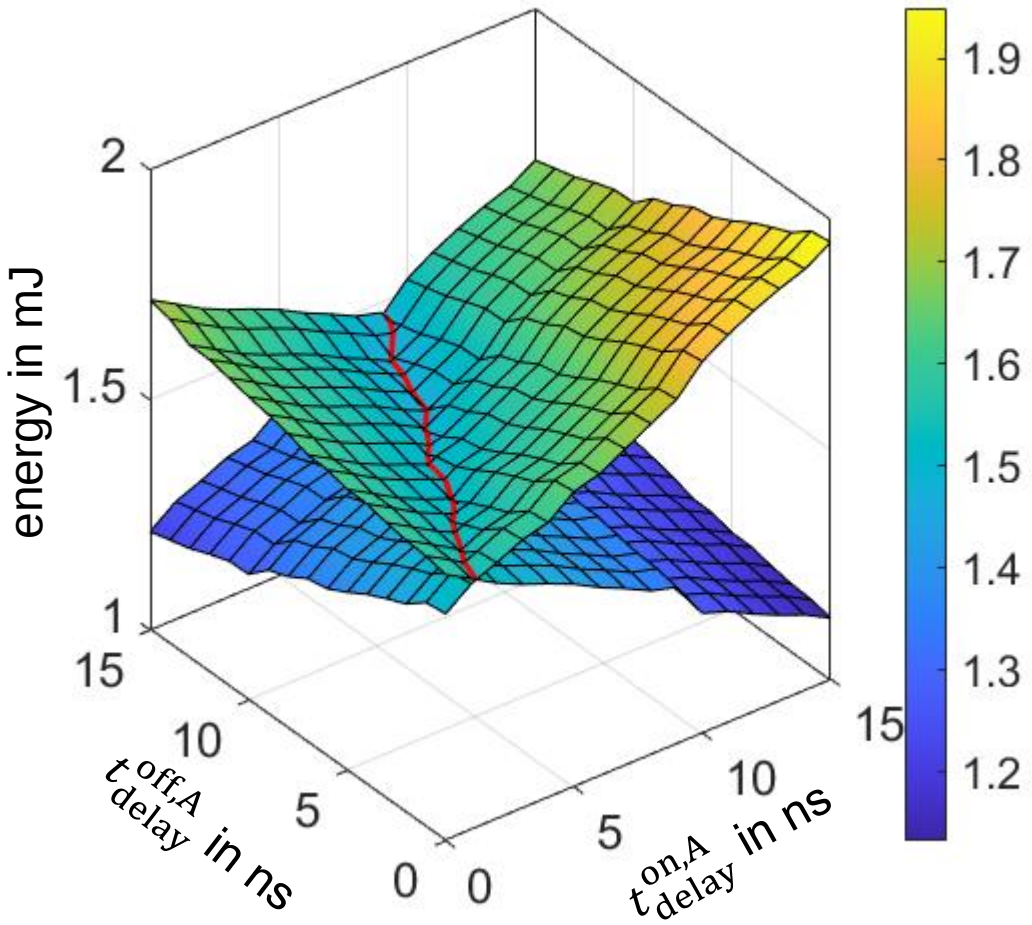
Conclusions & Outlook

- Proposed driver can freely shift the switching losses between parallel MOSFETs
- Highly beneficial for MOSFETs with different thermal resistance with regard to the cooling system
- Equal aging of the MOSFETs can be achieved

- Influence of temperature and different operating points needs to be examined



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